Examiner's Amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Mr.Sean F. Sullivan (Registration number: 38,328) on 2/9/09.

3. The claims have been amended as follows:

1. A method of performing memory mapped input output operations to an alternate address space comprising:

establishing a first instruction directed to a first memory mapped input output alternate address space associated with an adapter to store data in accordance with resource address designation, said resource address designation configured for decomposition thereof such that said first memory mapped input output alternate address space associated with said adapter is accessible;

establishing a second instruction directed to said first memory mapped input output alternate address space associated with an adapter to load data in accordance with said resource address designation;

allocating, through a host program, at least one of a real resource and a virtual resource associated with said first memory mapped input output alternate address space to a guest program started by the host program;

ensuring that a process executed by the guest program corresponds to said at least one of the real resource and the virtual resource allocated to the guest program, in a manner that is not visible to the quest program; and

wherein said process issues at least one of said first instruction and said second instruction and thereby causes execution of at least one of said store and load with said first memory mapped input output alternate address space.

2. The method of Claim 1 further comprising allocating, through the host program on behalf of the guest program, an error storage area associated with said resource.

3. The method of Claim 1 further including virtualization of a resource of one of said adapter to store data and said adapter to load data to a second-level guest process.

4. The method of Claim 3 wherein said virtualization of a resource is accomplished and distinguished from a real resource by partitioning a range of resource identifiers into a plurality of portions;

wherein at least one portion corresponds to a virtual resource; and

wherein when at least one of said first instruction and said second instruction specifies a resource identifier corresponding to said at least one portion, the guest program issuing instruction exits, and the host program resumes execution in order to emulate said at least one of said first instruction and said second instruction originally issued by the guest program.

5. The method of claim 3 wherein said virtualization provides direct access to at least one of a real resource and a virtual resource of an adapter by a problem-state second -level guest process.

6. The method of claim 5 wherein said access is accomplished without involvement from a kernel of a guest operating system; and permits said process operating in a problem-state maximum efficiency in performing the primary input output capabilities provided by said adapter and the associated resources allocated to said process.

7. The method of claim 3 further including separating another process operating under said operating system; wherein an separating is established on a per-resource basis during said allocating and is enforced during execution of at least one of said first and said second instructions.

8. The method of claim 1 wherein said first alternate address space is not a portion of the main address space from which said process is executing.

9. The method of claim 1 wherein said process issuing said at least one of said first instruction and said second instruction and thereby causes execution of at least one of said store and load with said first alternate address space operates in a problem state of a machine.

10-11. Cancelled

12. The method of claim 1 wherein at least one of said first instruction and said second instruction is executed without supervisory state intervention.

13. The method of claim 1 wherein said first instruction and said second instruction are semiprivileged instructions that may be executed in a problem state, wherein ownership of a specified resource of a specified adapter determines a privilege required for execution of said semiprivileged instructions.

14. The method of claim 1 further including a second memory mapped input output alternate address space associated with a second adapter.

15. The method of claim 14 wherein a storage location in said first memory mapped input output alternate address space maps to a different address than the same location in said second memory mapped input output alternate address space.

16. The method of claim 1 wherein said adapter includes address spaces as partitions of said alternate address space.

17. The method of claim 1 wherein an address space is governed by at least one of a resource type and storage area types associated with said adapter.

18. Storage medium encoded with a computer-readable computer program code, said code including instructions, when executed, cause a computer to implement a method of performing memory mapped input output operations to an alternate address space, the method comprising:

establishing a first instruction directed to a first memory mapped input output alternate address space associated with an adapter to store data in accordance with resource address designation, said resource address designation configured for decomposition thereof such that said first memory mapped input output alternate address space associated with said adapter is accessible;

establishing a second instruction directed to said first memory mapped input output alternate address space associated with an adapter to load data in accordance with said resource address designation;

allocating, through a host program, at least one of a real resource and a virtual resource associated with said first memory mapped input output alternate address space to a guest program started by the host program;

ensuring that a process executed by the guest program corresponds to said at least one of the real resource and the virtual resource allocated to the guest program, in a manner that is not visible to the quest program; and

wherein said process issues at least one of said first instruction and said second instruction and thereby causes execution of at least one of said store and load with said first memory mapped input output alternate address space.

19. A system for performing memory mapped input output operations to an alternate address space comprising:

a processor;

a means for establishing a first instruction directed to a first memory mapped input output alternate address space associated with an adapter to store data in accordance with resource address designation, said resource address designation configured for decomposition thereof such that said first memory mapped input output alternate address space associated with said adapter is accessible;

a means for establishing a second instruction directed to said first memory mapped input output alternate address space associated with an adapter to load data in accordance with said resource address designation;

a means for allocating, through a host program, at least one of a real resource and a virtual resource associated with said first memory mapped input output alternate address space to a guest program started by the host program;

a means for ensuring that a process executed by the guest program corresponds to said at least one of the real resource and the virtual resource allocated to the guest program, in a manner that is not visible to the quest program; and

wherein said process issues at least one of said first instruction and said second instruction and thereby causes execution of at least one of said store and load with said first memory mapped input output alternate address space.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAMQUY TRUONG whose telephone number is (571)272-3773. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai An can be reached on (703)305-9678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/ Camquy Truong
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